

BUK75/7608-40B

N-channel TrenchMOS standard level FET

Rev. 03 — 28 November 2007

Product data sheet

1. Product profile

1.1 General description

N-channel enhancement mode field-effect power transistor in a plastic package using NXP High-Performance Automotive (HPA) TrenchMOS technology.

1.2 Features

- Very low on-state resistance
- 175 °C rated
- Q101 compliant
- Standard level compatible

1.3 Applications

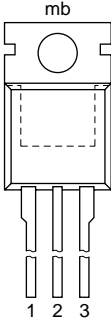
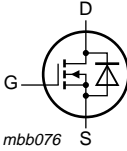
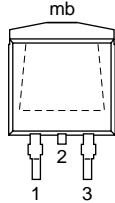
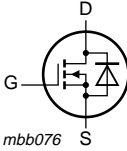
- Automotive systems
- Motors, lamps and solenoids
- General purpose power switching
- 12 V loads

1.4 Quick reference data

- $E_{DS(AL)S} \leq 241$ mJ
- $I_D \leq 75$ A
- $R_{DSon} = 6.6$ m Ω (typ)
- $P_{tot} \leq 157$ W

2. Pinning information

Table 1. Pinning - SOT78 and SOT404, simplified outlines and symbol

| Pin | Description | Simplified outline | Symbol |
|-----|---------------------------------------|--|---|
| 1 | Gate (G) |  |  |
| 2 | Drain (D) ^[1] | | |
| 3 | Source (S) | | |
| mb | mounting base, connected to drain (D) |  SOT404 (D2PAK) |  |

[1] It is not possible to make connection to pin 2 of the SOT404 package.

3. Ordering information

Table 2. Ordering information

| Type number | Package | | Version |
|-------------|----------|--|---------|
| | Name | Description | |
| BUK7508-40B | TO-220AB | plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB | SOT78A |
| BUK7608-40B | D2PAK | plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) | SOT404 |

4. Limiting values

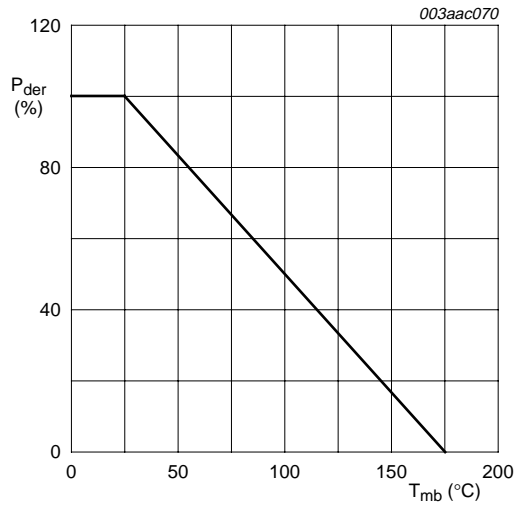
Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit | |
|-----------------------------|--|---|-----|----------|------------------|---|
| V_{DS} | drain-source voltage | | - | 40 | V | |
| V_{DGR} | drain-gate voltage (DC) | $R_{GS} = 20 \text{ k}\Omega$ | - | 40 | V | |
| V_{GS} | gate-source voltage | | - | ± 20 | V | |
| I_D | drain current | $T_{mb} = 25 \text{ }^\circ\text{C}$; $V_{GS} = 10 \text{ V}$; see Figure 2 and 3 | [1] | - | 101 | A |
| | | | [2] | - | 75 | A |
| | | $T_{mb} = 100 \text{ }^\circ\text{C}$; $V_{GS} = 10 \text{ V}$; see Figure 2 | [1] | - | 71 | A |
| I_{DM} | peak drain current | $T_{mb} = 25 \text{ }^\circ\text{C}$; pulsed; $t_p \leq 10 \text{ }\mu\text{s}$; see Figure 3 | - | 407 | A | |
| P_{tot} | total power dissipation | $T_{mb} = 25 \text{ }^\circ\text{C}$; see Figure 1 | - | 157 | W | |
| T_{stg} | storage temperature | | -55 | +175 | $^\circ\text{C}$ | |
| T_j | junction temperature | | -55 | +175 | $^\circ\text{C}$ | |
| Source-drain diode | | | | | | |
| I_{DR} | reverse drain current | $T_{mb} = 25 \text{ }^\circ\text{C}$ | [1] | - | 101 | A |
| | | | [2] | - | 75 | A |
| I_{DRM} | peak reverse drain current | $T_{mb} = 25 \text{ }^\circ\text{C}$; pulsed; $t_p \leq 10 \text{ }\mu\text{s}$ | - | 407 | A | |
| Avalanche ruggedness | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | unclamped inductive load; $I_D = 75 \text{ A}$; $V_{DS} \leq 40 \text{ V}$; $V_{GS} = 10 \text{ V}$; $R_{GS} = 50 \text{ }\Omega$; starting at $T_{mb} = 25 \text{ }^\circ\text{C}$ | - | 241 | mJ | |

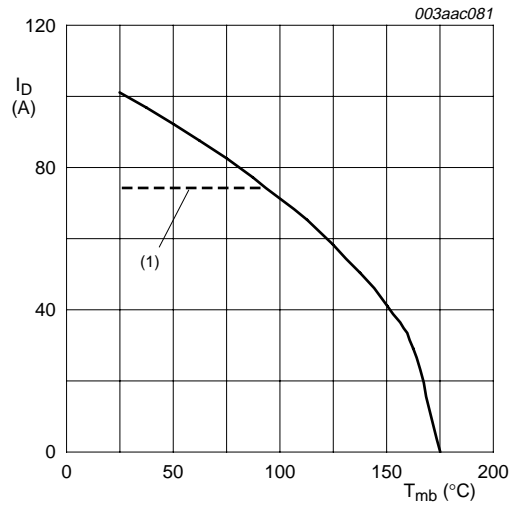
[1] Current is limited by power dissipation chip rating.

[2] Continuous current is limited by package.



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

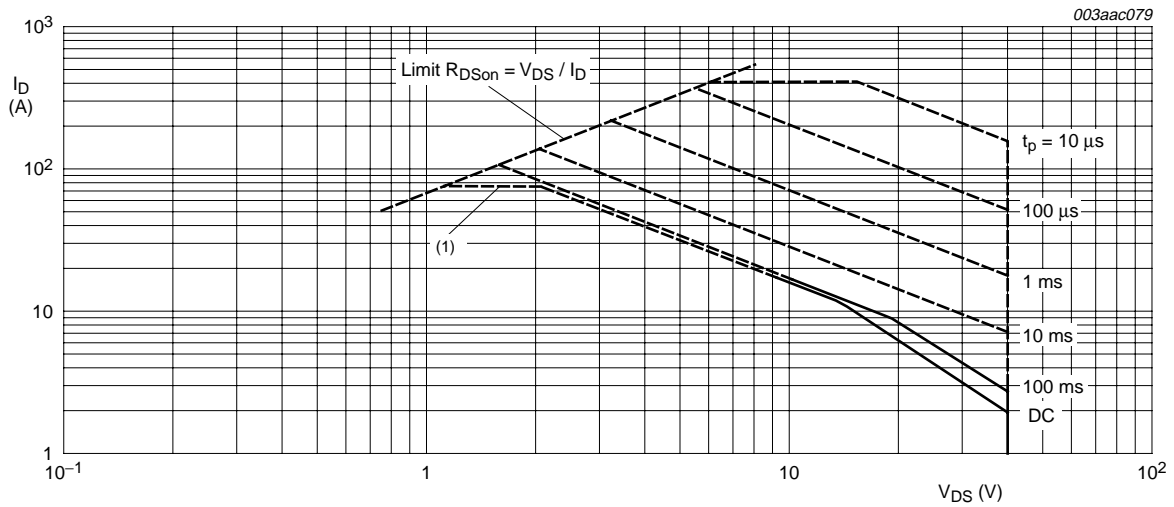
Fig 1. Normalized total power dissipation as a function of solder point temperature



V_{GS} ≥ 10 V

[1] Capped at 75 A due to package.

Fig 2. Continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is single pulse.

[1] Capped at 75 A due to package.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|----------------|---|------------------------------|-----|-----|------|------|-----|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | see Figure 4 | - | - | 0.95 | K/W | |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | | [1] | - | 60 | - | K/W |
| | | | [2] | - | 50 | - | K/W |

[1] Vertical in still air; SOT78 package.

[2] mounted on a printed circuit board; minimum footprint; SOT404 package

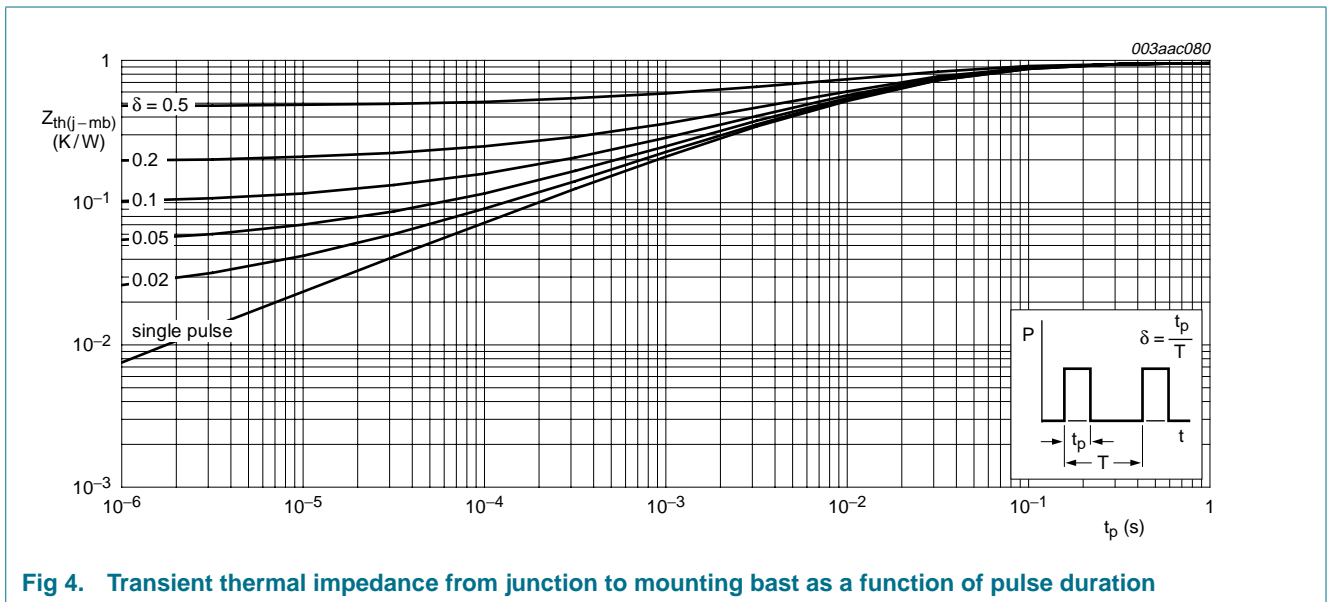


Fig 4. Transient thermal impedance from junction to mounting bast as a function of pulse duration

6. Characteristics

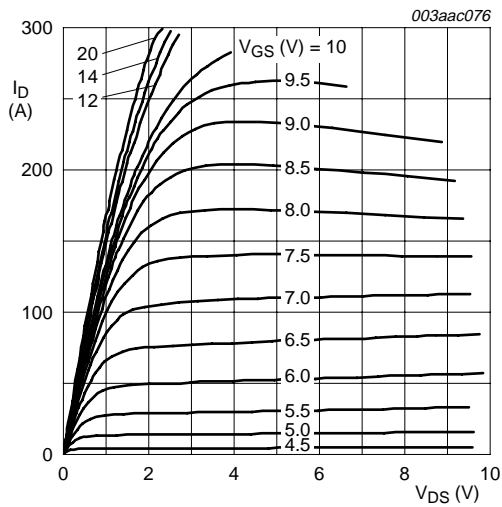
Table 5. Characteristics

$T_j = 25\text{ °C}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|----------------------------------|---|-----|------|------|---------------|
| Static characteristics | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D = 250\ \mu\text{A}; V_{GS} = 0\ \text{V}$ | | | | |
| | | $T_j = 25\text{ °C}$ | 40 | - | - | V |
| | | $T_j = -55\text{ °C}$ | 36 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D = 1\ \text{mA}; V_{DS} = V_{GS};$ see Figure 9 and 10 | | | | |
| | | $T_j = 25\text{ °C}$ | 2 | 3 | 4 | V |
| | | $T_j = 175\text{ °C}$ | 1 | - | - | V |
| | | $T_j = -55\text{ °C}$ | - | - | 4.4 | V |
| I_{DSS} | drain leakage current | $V_{DS} = 40\ \text{V}; V_{GS} = 0\ \text{V}$ | | | | |
| | | $T_j = 25\text{ °C}$ | - | 0.02 | 1 | μA |
| | | $T_j = 175\text{ °C}$ | - | - | 500 | μA |
| I_{GSS} | gate leakage current | $V_{GS} = \pm 20\ \text{V}; V_{DS} = 0\ \text{V}$ | - | 2 | 100 | nA |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = 10\ \text{V}; I_D = 25\ \text{A};$ see Figure 6 and 8 | | | | |
| | | $T_j = 25\text{ °C}$ | - | 6.6 | 8 | m Ω |
| | | $T_j = 175\text{ °C}$ | - | - | 15.2 | m Ω |
| Dynamic characteristics | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D = 25\ \text{A}; V_{DD} = 32\ \text{V}; V_{GS} = 10\ \text{V};$ see Figure 14 | - | 36 | - | nC |
| Q_{GS} | gate-source charge | | - | 9 | - | nC |
| Q_{GD} | gate-drain charge | | - | 12 | - | nC |
| C_{iss} | input capacitance | $V_{GS} = 0\ \text{V}; V_{DS} = 25\ \text{V}; f = 1\ \text{MHz};$ see Figure 12 | - | 2017 | 2689 | pF |
| C_{oss} | output capacitance | | - | 486 | 583 | pF |
| C_{rss} | reverse transfer capacitance | | - | 213 | 291 | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DD} = 30\ \text{V}; R_L = 1.2\ \Omega;$ | - | 20 | - | ns |
| t_r | rise time | $V_{GS} = 10\ \text{V}; R_G = 10\ \Omega$ | - | 51 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 20 | - | ns |
| t_f | fall time | | - | 33 | - | ns |
| L_D | internal drain inductance | from drain lead 6 mm from package to center of die | - | 4,5 | - | nH |
| | | from contact screw on mounting base to center of die SOT78 | - | 3.5 | | nH |
| | | from upper edge of drain mounting base to center of die SOT404 | - | 2.5 | - | nH |
| L_S | internal source inductance | from source lead 6 mm from package to source bond pad | - | 7.5 | - | nH |

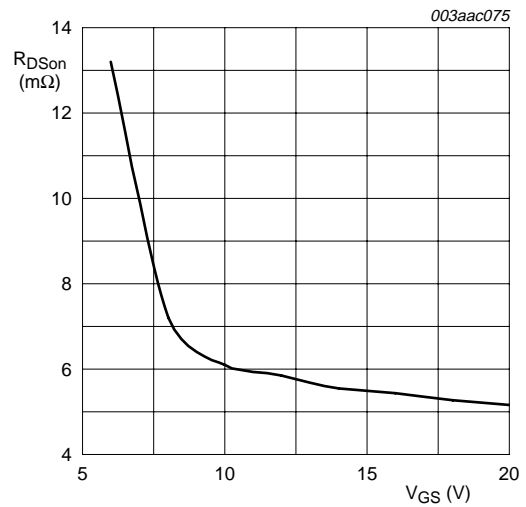
Table 5. Characteristics ...continued
 $T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------------|-----------------------|---|-----|------|-----|------|
| Source-drain diode | | | | | | |
| V_{SD} | source-drain voltage | $I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; see Figure 15 | - | 0.85 | 1.2 | V |
| t_{rr} | reverse recovery time | $I_S = 20\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = -10\text{ V}$; $V_{DS} = 20\text{ V}$ | - | 53 | - | ns |
| Q_r | recovered charge | | - | 44 | - | nC |



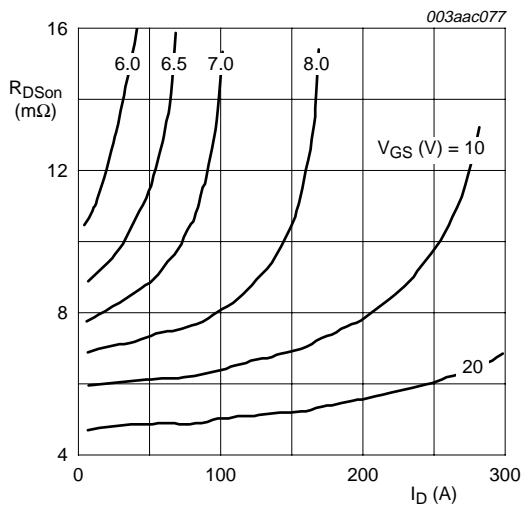
$T_j = 25\text{ }^\circ\text{C}$; $t_p = 300\text{ }\mu\text{s}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



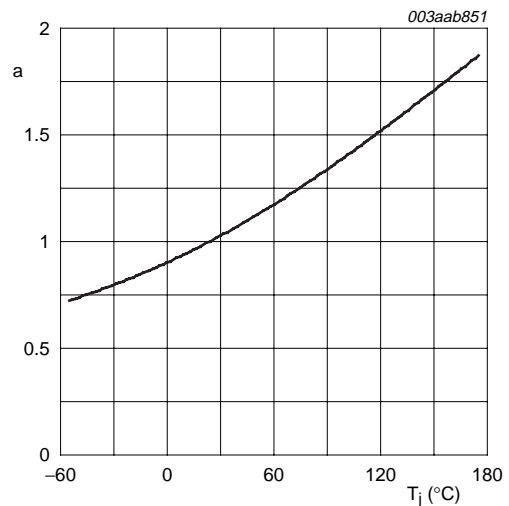
$T_j = 25\text{ }^\circ\text{C}$; $I_D = 25\text{ A}$

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values



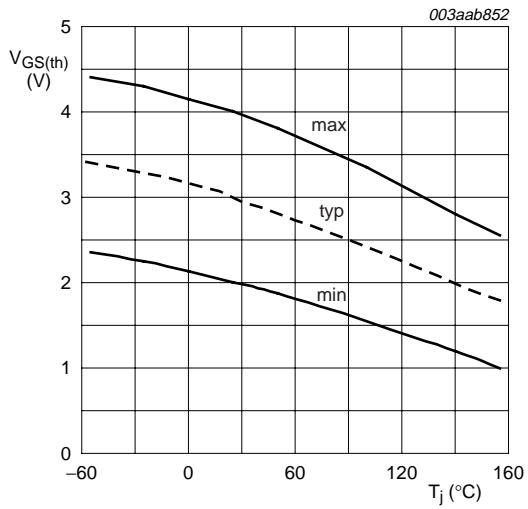
$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



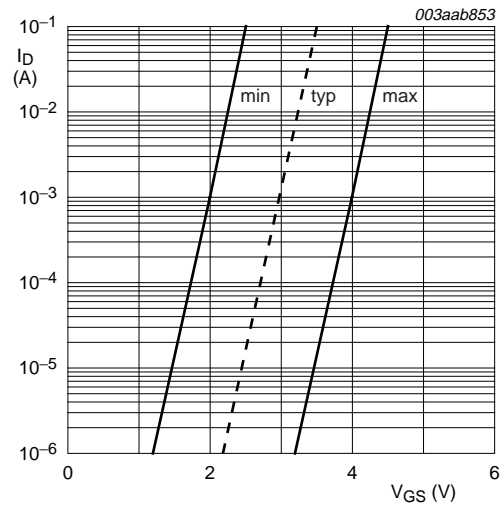
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



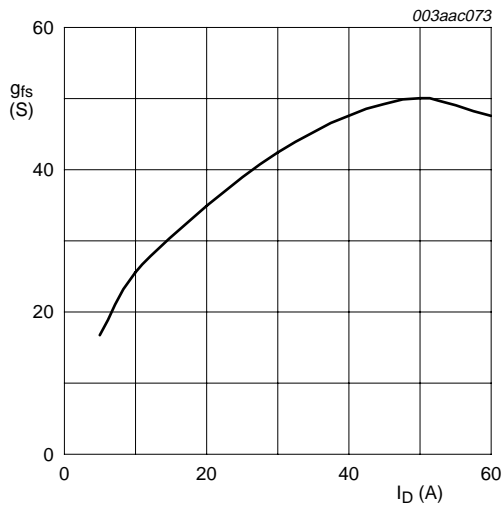
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



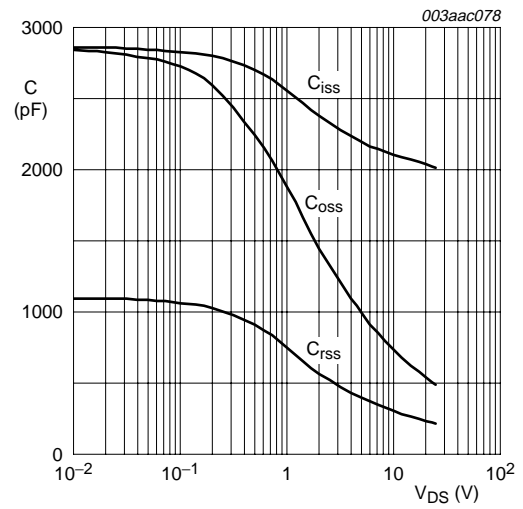
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 25 \text{ V}$

Fig 11. Forward transconductance as a function of drain current; typical values.



$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.

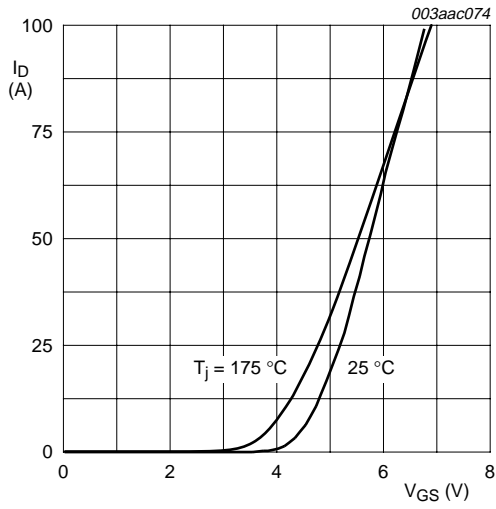


Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values

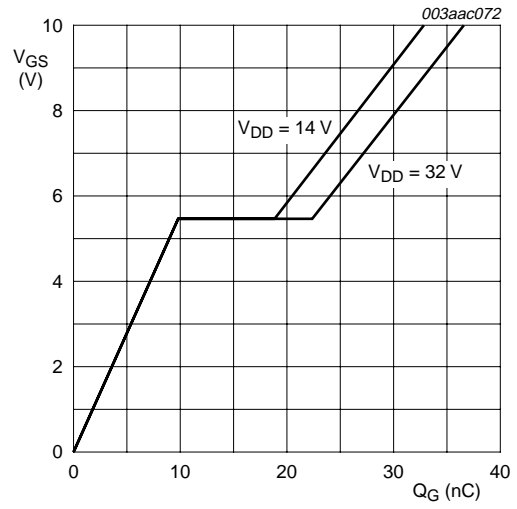


Fig 14. Gate-source voltage as a function of turn-on gate charge; typical values.

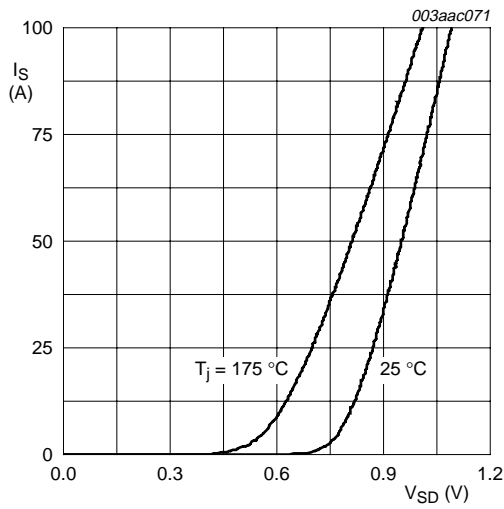


Fig 15. Reverse diode current as a function of reverse diode voltage; typical values

7. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78A

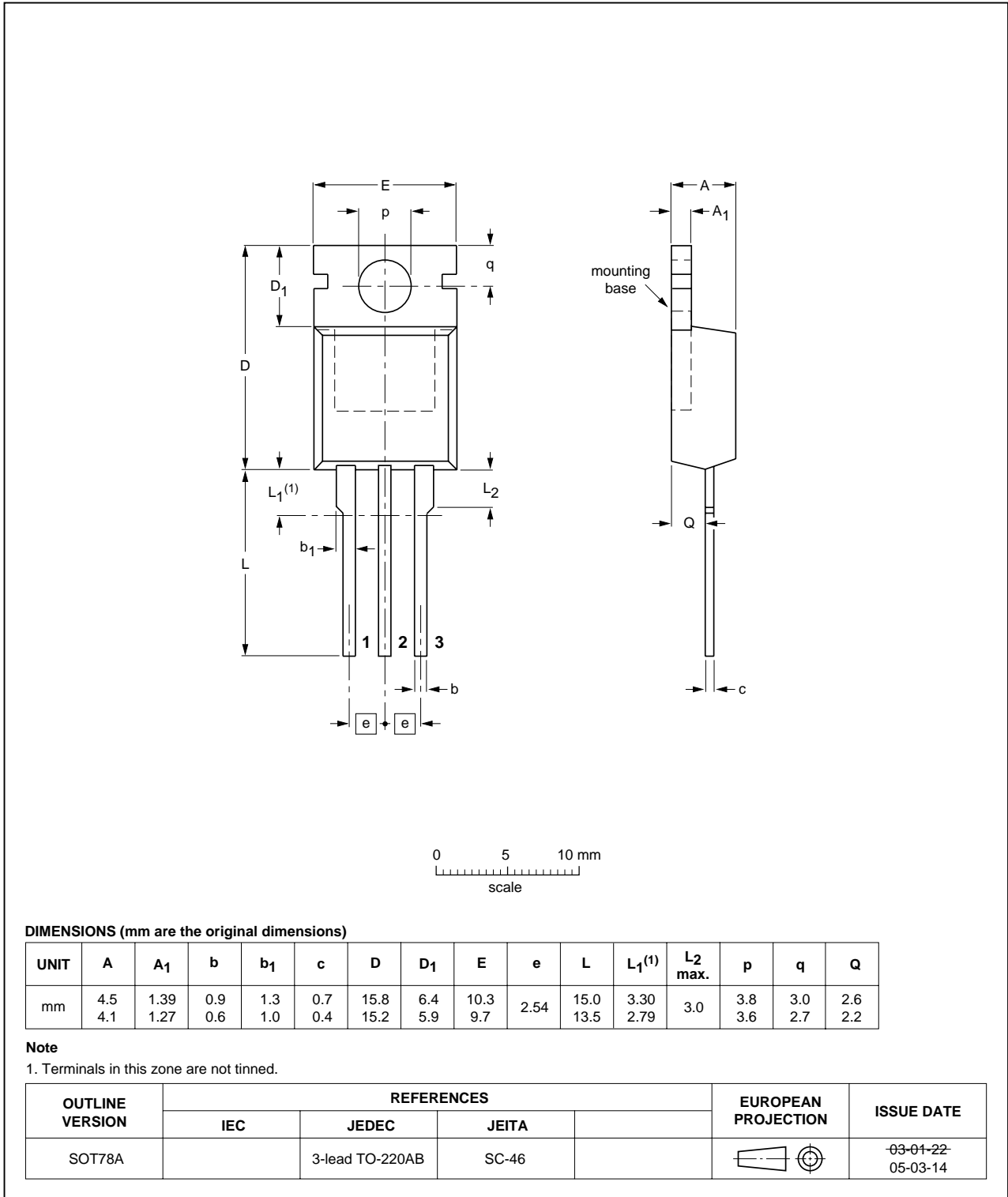


Fig 16. Package outline SOT78A (TO-220AB)

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404

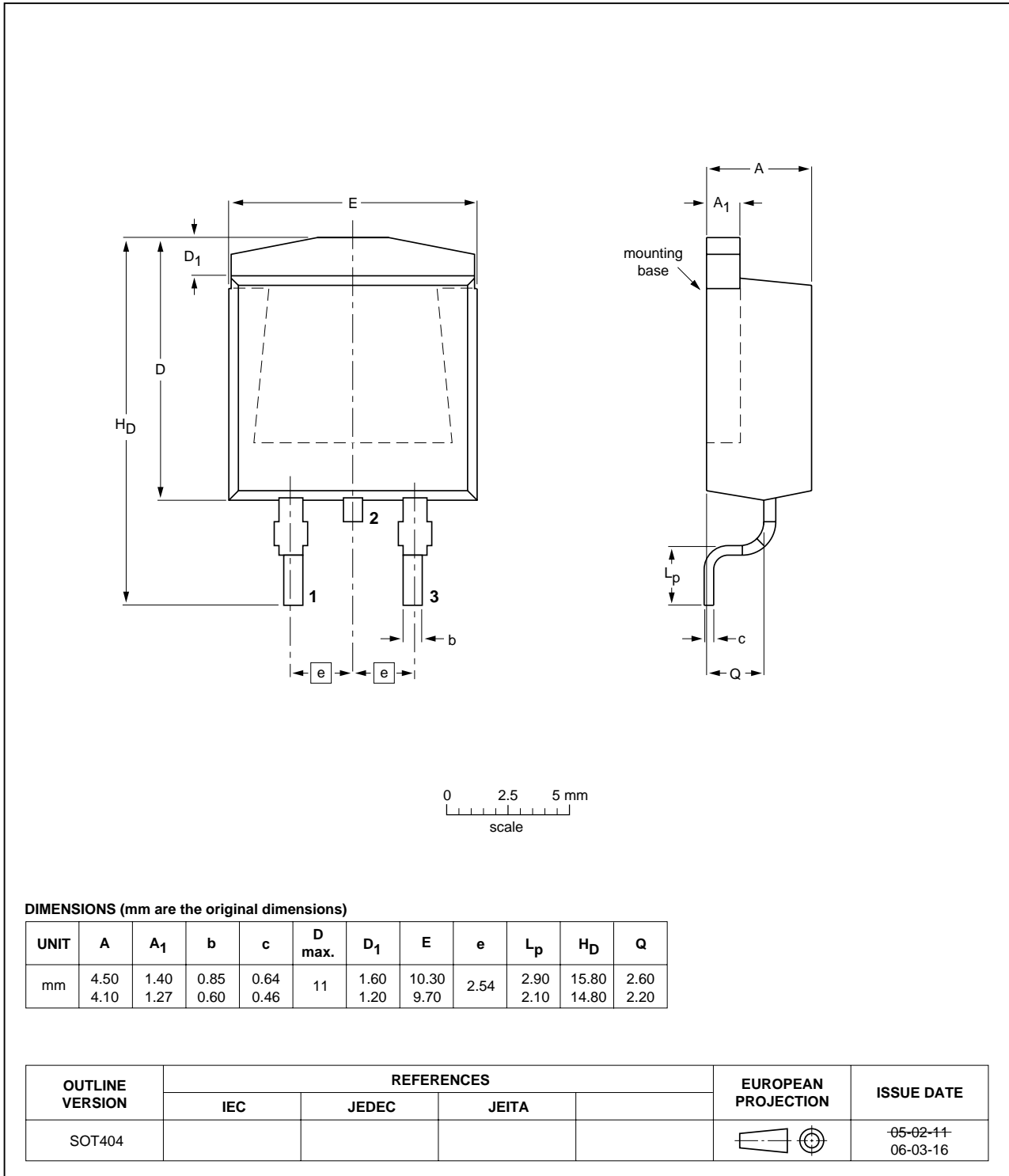
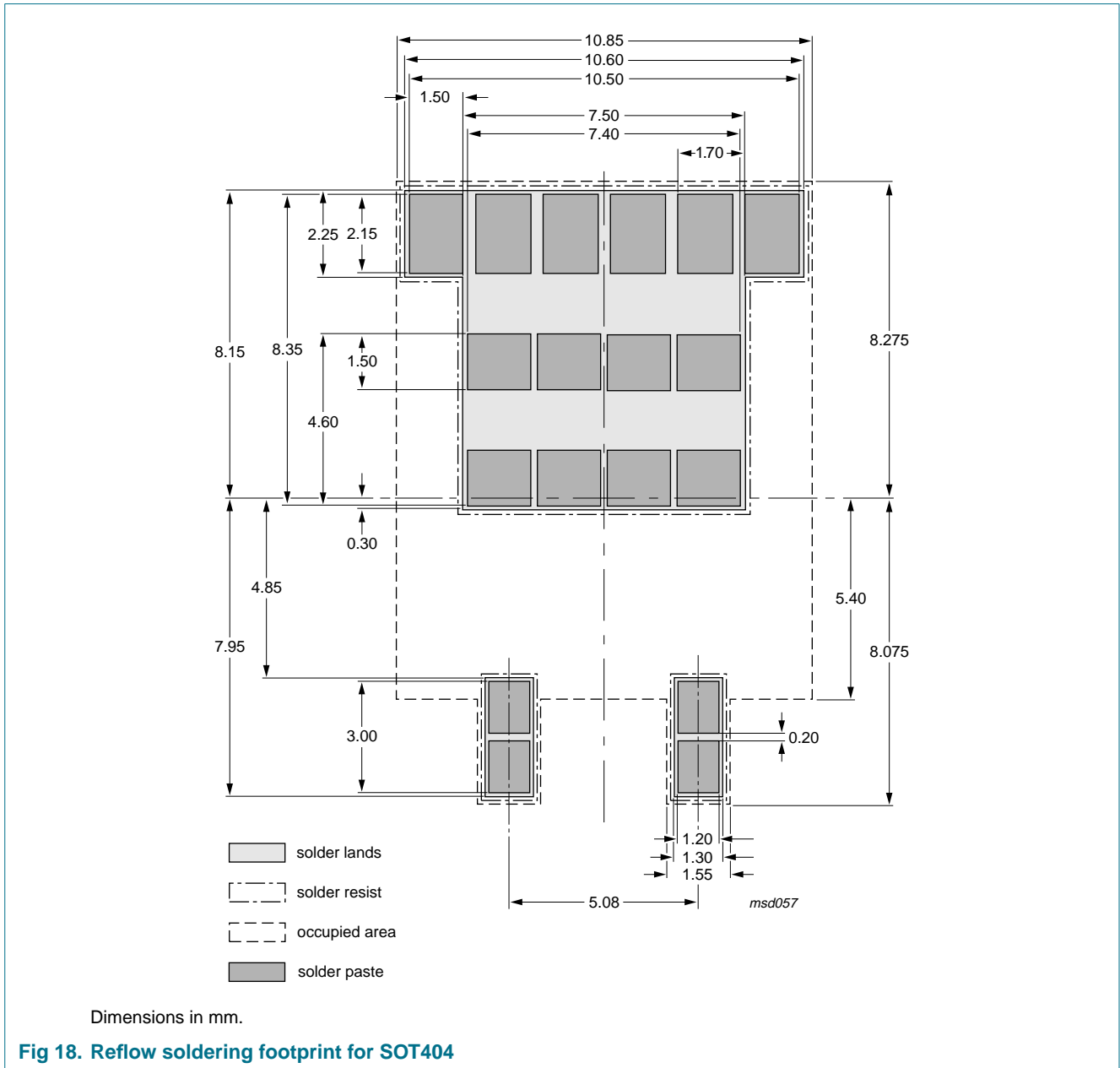


Fig 17. Package outline SOT404 (D2PAK)

8. Soldering



9. Revision history

Table 6. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-------------------|--|--------------------|---------------|-------------------|
| BUK75_7608-40B_3 | 20071128 | Product data sheet | - | BUK75_7608-40B_2 |
| Modifications: | <ul style="list-style-type: none">• The format of this data sheet has been redesigned to correct a layout error. | | | |
| BUK75_7608-40B_2 | 20071116 | Product data sheet | - | BUK75_7608_40B-01 |
| Modifications: | <ul style="list-style-type: none">• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.• Legal texts have been adapted to the new company name where appropriate. | | | |
| BUK75_7608_40B-01 | 20030319 | Product data sheet | - | - |

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| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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Date of release: 28 November 2007

Document identifier: BUK75_7608-40B_3